3W, Q BAND SOLID STATE AMPLIFIER

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by

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ABSTRACT

The design of Q band IMPATT diode cavity combiners is discussed. The design is based on a three-step closed form algorithm. The first step is the characterization of the passive circuit (cavity and diode package) using an automatic network analyzer. In the second step, a computer program is used to generate diode device lines. The third step is the load line synthesis for predictable operation as either an injection-locked oscillator or a stable negative resistance amplifier. These procedures were used to design a three-diode, two-stage amplifier using 2-watt, 44-GHz GaAs IMPATT diodes. An output power of 3 watts with 11 dB gain was achieved.

1.0 INTRODUCTION

Over 2 watts CW has been obtained at 44 GHz simultaneously with a conversion efficiency of 17 percent and a thermal resistance of less than 21° C/W, from a double-drift, Read profile gallium arsenide IMPATT diode developed at the Research Division of Raytheon Company.

Obtaining predictable and repeatable Q band amplifier performance using this IMPATT diode is a challenging task, due to the high operating frequency and the low diode impedance. Actually, the design of high-power IMPATT diode circuits, at any frequency, is not a trivial matter. These two-terminal devices present a negative resistance over a broad frequency range, and their impedance, which must be matched by the circuit, is very low. They are, therefore, difficult to control. One can empirically obtain an occasional impressive result; however, for predictable and repeatable operation, sound design procedures must be used. Such procedures have been developed and successfully used from C to Ku Band[1]. Presently, their application to the design of Q Band rectangular cavity power combiners is discussed.

2.0 DESIGN PROCEDURES

The cavity power combining approach is shown schematically in Fig. 1a. The diodes are mounted in coaxial lines which are magnetically coupled to a cavity resonating in the TE_{10n} mode. For the two-diode case shown in Fig. 1a, n = 1; for a four-diode combiner, n = 2; and for M diodes, n = M/2.

Amplifier design can be divided conveniently into three parts: (1) design of the cavity circuit, (2) IMPATT diode characterization, and (3) the design of a network which matches the two.

The objective of the circuit represented in Fig. 1b is to combine the rf power incident on ports AA and BB into the load, R_L, at the design frequency. At all other frequencies, the incident power should be dissipated in the loads R_O. To accomplish this, the cavity impedance, "seen" at the input ports AA and BB, must be real at the design frequency and much larger than R_O. At all other frequencies, the cavity impedance is very small, so R_O is the dominant factor.

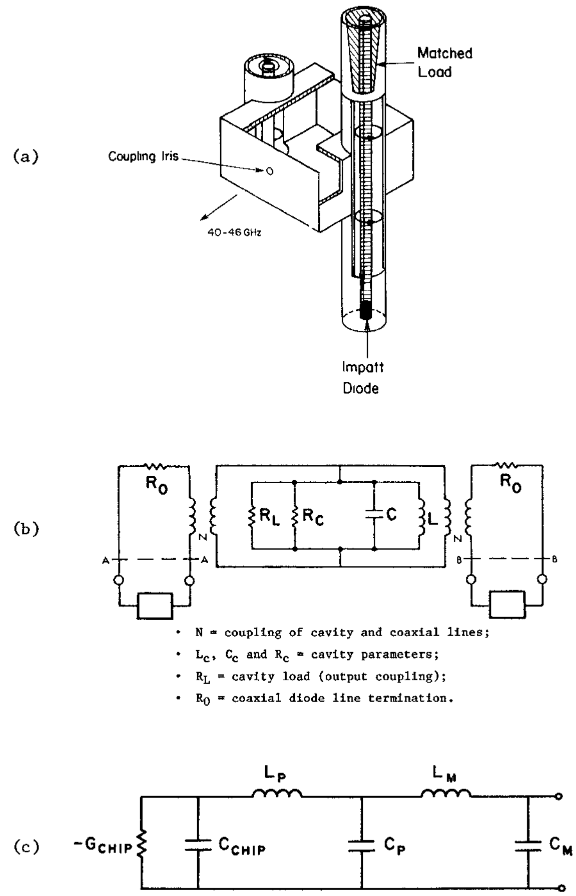

Figure 1. Resonant cavity approach, equivalent circuits and physical principles: a) Rectangular waveguide cavity combiner; b) Equivalent circuit near cavity resonant frequency; c) Diode/package equivalent circuit.

The next design requirement is to ensure that the IMPATT diodes generate their maximum power for combining in the circuit. This is accomplished with a matching network which transforms the impedances at planes AA and BB in such a way that each IMPATT diode operates at the design frequency, either as an amplifier at the desired gain and output power or as an oscillator at maximum power.

A diode equivalent circuit is shown in Fig. 1c, and measured values for diode impedance in a 2-GHz band are shown in Fig. 2. The negative of the diode impedance ($-Z_{diode} > 0$) is shown for both a packaged and an unpackaged diode, on a 15-ohm Smith chart, as a function of the rf voltage arose the diode for three discrete frequencies, (F_o-1) GHz, F_o, and (F_o+1) GHz, where F_o = 44.5 GHz.

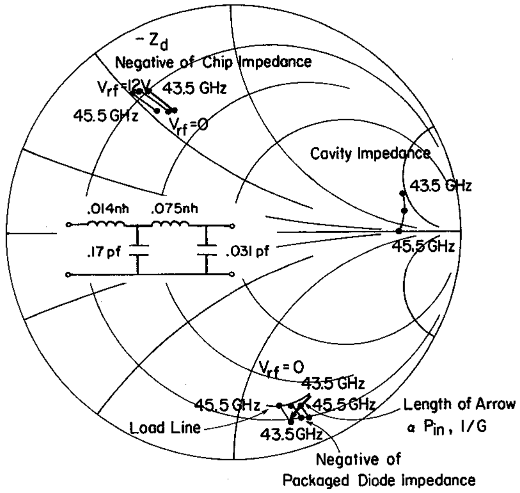

Figure 2. Circuit/diode matching for amplifier operation (15 ohm impedance chart).

The cavity impedance (impedance at points AA and BB in Fig. 1b) for a two-diode combiner is also shown for the same frequency range. If the cavity impedance is transformed in such a way that the resulting impedance locus (the load line) intersects the negative of the diode impedance at some common frequency, the circuit operates as an oscillator at that frequency. The oscillator output power varies according to the exact position of the intersection. If the intersection occurs in the larger V_{rf} region (~10-12 volts), maximum power is obtained (2 watt, CW). As the intersection moves toward 0 volts V_{rf}, the oscillator power drops. In this case, an input signal may be provided to "connect" (in Fig. 2) the large V_{rf} points with the load line (at the same frequency, of course). This situation corresponds to amplifier operation. The further the load line is located from the diode's maximum power point, the larger the input signal must be to "bridge" this distance, and hence, the lower the amplifier gain will be (for maximum added power). For the diode-cavity match shown in Fig. 2, the relative position of the load line and the diode impedance was such that the circuit performed as a negative resistance amplifier. Three watts output power and 5 dB gain were obtained at band center. Z_{load} for the packaged diode barely touched the diode impedance at 44.5 GHz and $V_{rf} \approx 0$ volts, and hence, without an input signal, the added power was insignificant.

Therefore, to obtain predictable performance, it is necessary to know the negative of the diode impedance and to control the impedance presented to each diode.

Diode impedance data can be generated by a computer model and/or measured in the laboratory. Computer modeling has the advantage of speed, but its validity must be confirmed by measurement for each diode type, frequency, and rf power range. The data shown in Fig. 2 were generated by computer and validated in the laborabory. The package equivalent circuit was determined experimentally using an automatic network analyzer to measure the circuit elements.

The cavity combiner has also been characterized and optimized using the automatic network analyzer. Once the combiner has been characterized, it can be appropriately matched to the diodes with a single section transformer.

Lumped element equivalent circuits for a cavity combiner like that shown in Fig. 1b are frequently used to predict and analyze combiner performance. However, a more accurate method has been developed and is presently employed for combiner characterization and optimization. This method utilizes a scattering matrix representation.

An automatic network analyzer is used to characterize the cavity combiner alone (without diodes). The diodes are replaced with short circuits and the reflection coefficient from the cavity's output port is measured. By repeating this measurement for at least three short positions, the complete S matrix is obtained[2,3]. From the S matrix, the cavity efficiency and the impedance presented to the diode ports are determined.

This method of combiner characterization is superior to the lumped element approach because, instead of making measurements on a combiner with one diode line and extrapolating the results to the multiple line case (introducing inaccuracies), it measures and computes loss and impedance for the multiple diode line combiner directly. Also, it allows one to measure iteratively the combiner loss and to adjust output coupling in order to maximize combiner efficiency and bandwidth. Once the combiner has been adjusted for minimum loss (or desired bandwidth), the diode line impedances in the multidiode environment are measured and used to design a matching transformer to obtain the performance required.

The accuracy with which a combiner can be characterized is shown in Figs. 3a and 3b. Shown are efficiency (the ratio of the power dissipated in R_L to the total power entering ports AA and BB, Fig. 1b) and diode line impedance (at ports AA and BB, Fig. 1b). A family of these curves is shown indicating: (1) repeatability of measurements during a single session; (2) repeatability after cavity disassembly and reassembly; and (3) repeatability of measurement performed on different days after the equipment has been recalibrated.

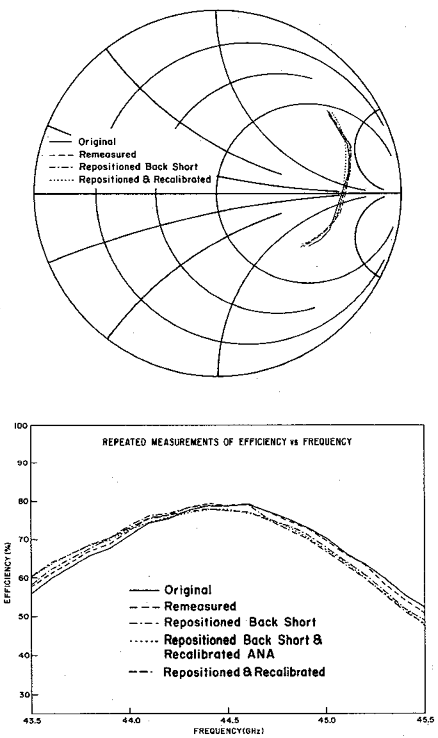

Figure 3. Repeated measurements of midplane impedance (50 Ω chart).

Excellent agreement has been obtained. This agreement is remarkable considering the frequency and the associated sensitivity to mechanical tolerances and assembly. Minor differences in assembly, like tightening screws, would show as large changes in combiner characteristics. Because these measurements are computer controlled, they could be easily incorporated into a production line check for cavity quality.

3.0 PERFORMANCE

The above method has been applied in the optimization of the TE_{101} cavity parameters shown in Fig. 1b.

For a two-diode cavity, resonating in the TE_{101} mode, the resulting combiner efficiency and diode line impedance as a function of coupling iris size are shown in Fig. 4a and 4b. To realize the efficiency shown in Fig. 4a, the signals at each of the diode ports must be of equal amplitude and phase. In practice, some additional losses are introduced because of differences in diode characteristics and mechanical tolerances. Hence, Fig. 4a shows the highest efficiency achievable when the combiner is operated as an oscillator. On the other hand, when the combiner is operated as an amplifier, there are two signals at each port: one incident toward the diode and the reflected amplifier signal. If the phasing of these two signals is properly adjusted, it has been shown[2] that the loss in the terminating loads can be reduced

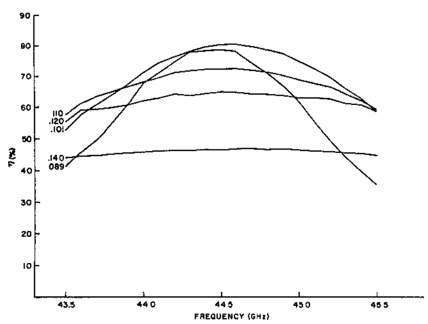

Figure 4a. Efficiency vs. frequency for two-diode combiner.

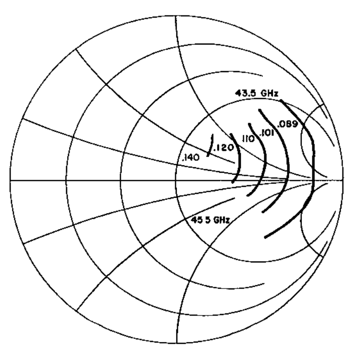

Figure 4b. Midplane impedance vs. iris (50 ohm impedance chart).

and a higher circuit efficiency can be achieved than the one shown in Fig. 4a. For amplifier operation, the efficiencies shown are minima. It can be seen from Fig. 4a that the maximum combiner efficiency increases as the coupling iris diameter is increased from 0.089 in. to 0.101 in. and then decreases with further increase of the iris. For a small diameter iris (0.089 in.), the loss in the cavity walls dominates. For a large iris (0.140 in.), it is the loss in the terminating loads which dominates.

It can also be seen from Figs. 4a and 4b that as the iris size increases, broader bandwidth can be achieved. First, the efficiency flattens over the band. Secondly, the variation of the cavity impedance with frequency is reduced for larger irises. This results in shorter load lines and flatter gains, but there is a practical limit to the maximum iris size that can be used because of the decrease in circuit efficiency. It is also difficult to obtain gains in excess of 5 dB with a very large iris due to the large impedance transformation requirement between the cavity and the diode. As the iris size increases, the cavity impedance "moves" toward the center of the Smith chart (Fig. 4b) and hence one needs a lower impedance transformer to match the diode. Five to 8 ohm transformers are the minimum that can be practically made.

A single diode circuit was designed in a manner similar to the two-diode case. Then both stages were integrated with circulators and assembled into a two-stage amplifier. The resulting amplifier performance (and block diagram) is shown in Fig. 5. Three watts and ~11 dB gain were obtained at 44.5 GHz. Two watts output power over 1 GHz band was also achieved. The power and gain dropped to 1 watt and 6 dB at the band edges. In order to increase the gain at the band edges, the load variation with frequency has to be reduced and its intersection with the diode impedance (Fig. 2) moved toward higher V_{rf}. Progress in this direction is shown as the dashed line in Fig. 5. Two watts output power over 1.3 GHz band (30 percent increase) were obtained while still preserving 3 watts at band center.

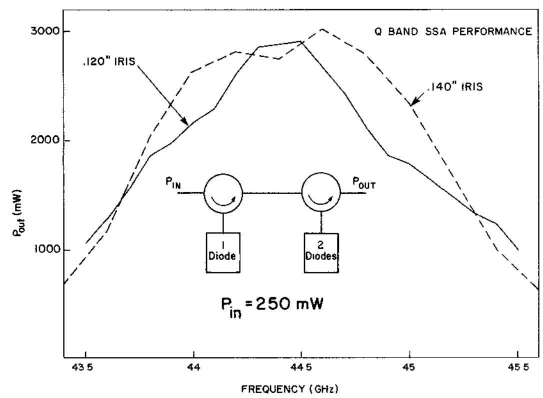

Figure 5. Q-band SSA performance and block diagram.

4.0 ACKNOWLEDGEMENTS

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5.0 REFERENCES

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